LAB 01: Half Adder

**Due: September 12**

# Purpose: In this project you are asked to define and test a Half Adder

# Objectives:

* **Continue to get familiar with EDAPlayground**
* **Start to learn HDL (Verilog) basics**
* **To understand binary addition**

**Step 1:** create module on the right panel

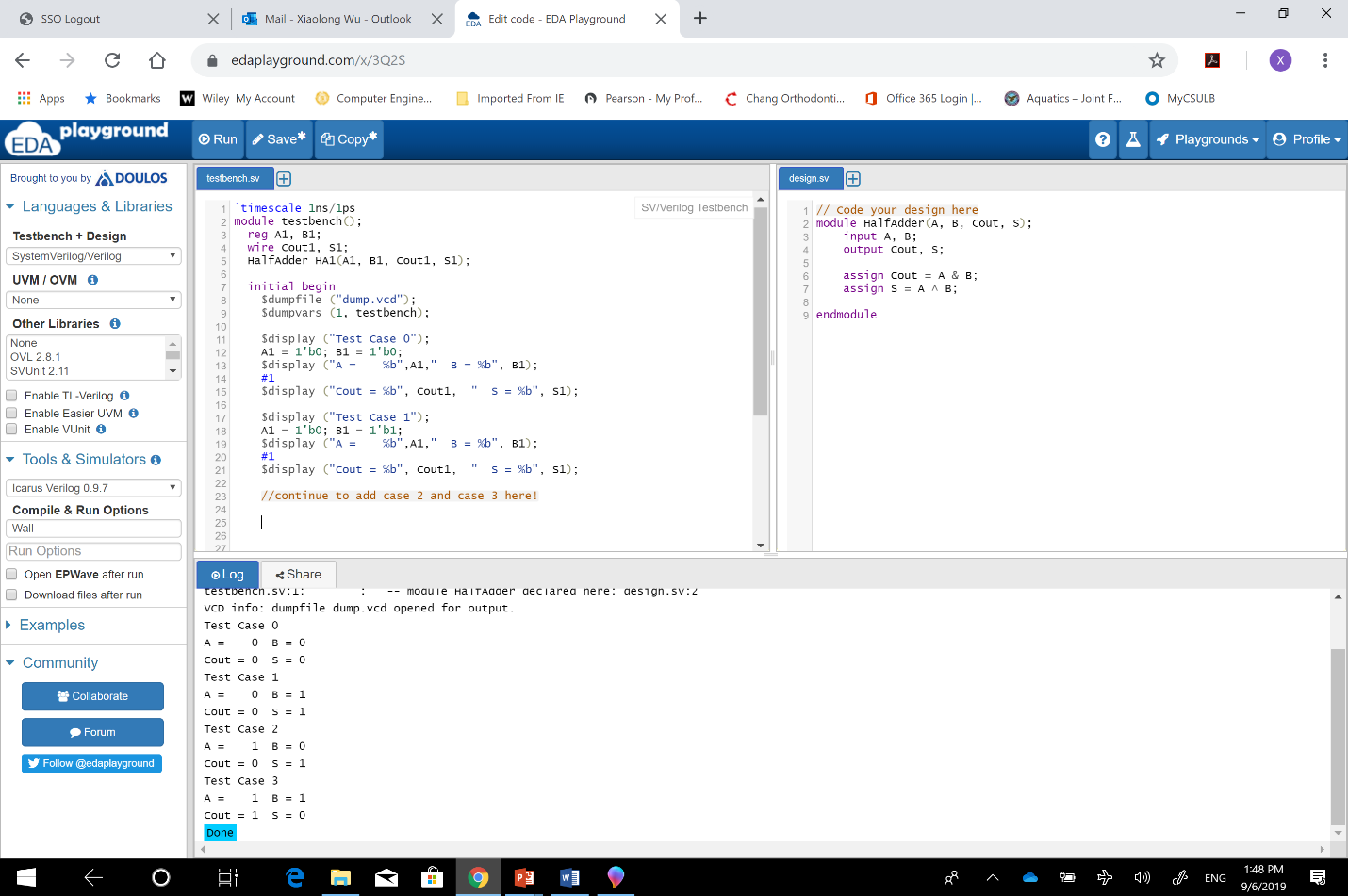
The Half Adder is a digital building block with 2 inputs (A, B) and 2 outputs (S, Cout). The Half Adder logic must be modeled next. The circuit below shows the Half Adder logic circuit and the equivalent boolean equations:

|  |  |
| --- | --- |
| out | **S = A xor B**  **Cout = A and B** |

**Binary Operator Symbols in Verilog**

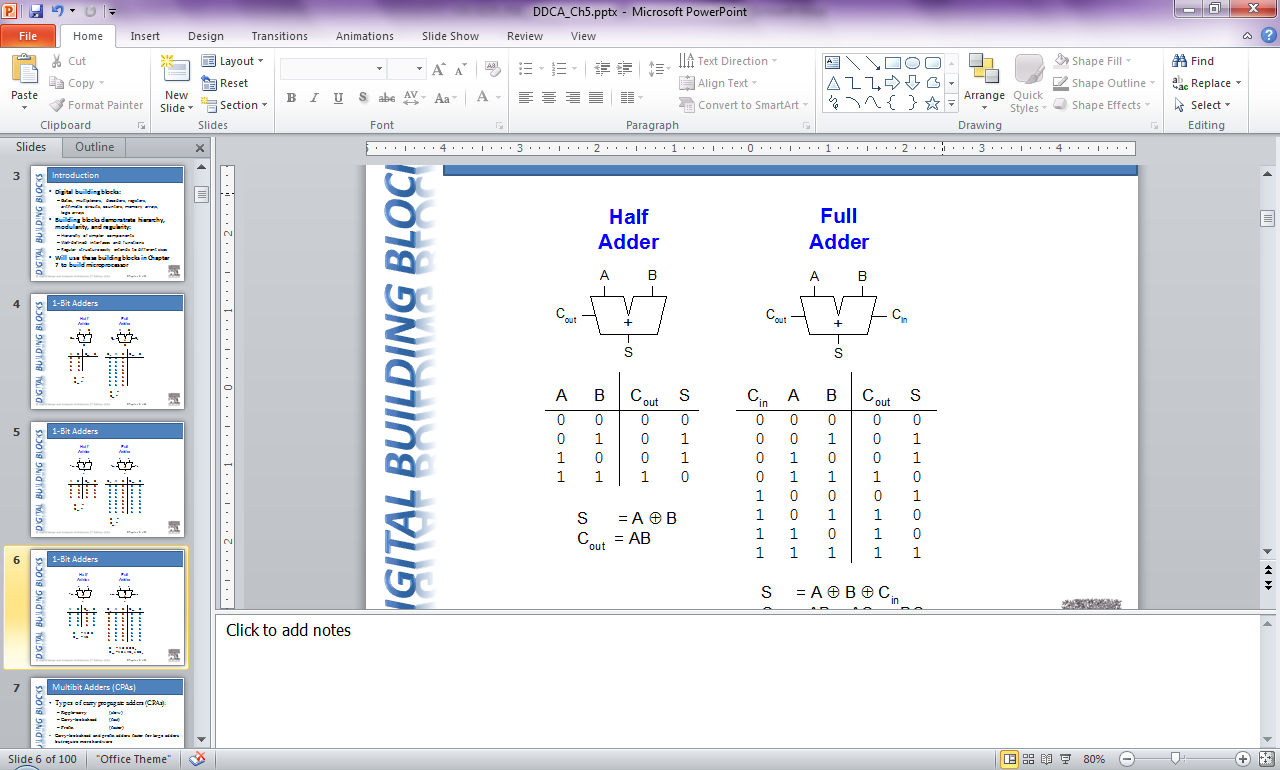
|  |  |
| --- | --- |
| ~ | NOT |
| \*, /, % | mult, div, mod |
| +, - | add,sub |
| <<, >> | shift |
| <<<, >>> | arithmetic shift |
| <, <=, >, >= | comparison |
| ==, != | equal, not equal |
| &, ~& | AND, NAND |
| ^, ~^ | XOR, XNOR |
| |, ~| | OR, NOR |
| ?: | ternary operator |

This completes the verilog module definition of the half adder. Next it must be tested to ensure it works correctly.



**Step 2:** **Create a Half Adder Verilog Test Fixture.** To test a module for correct functionality, a set of inputs will be provided to produce an expected set of outputs. A **Verilog Testbench** is used to test a Verilog source module.

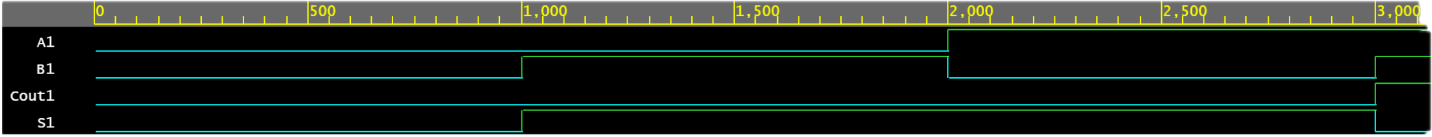
**Create the Half Adder test script.** To test a module for correct functionality, a set of inputs will be provided to produce an expected set of outputs. For simple modules like the half adder a truth table is used to show the outputs that can be expected from a set of inputs.



The Cout output column shows that Cout equals 1 only when A equals 1 and B equals 1.

The S output column shows that S equals 1 when the value of A is not equal to the value of B.

Simulation results are shown as waveforms.



**Finally**, upload report to the project Dropbox in beachboard (refer to EDAPlayground Tutorial for report guidance)!